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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

NEGRON, WANDA M

ART UNIT	PAPER NUMBER
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2622

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10/26/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/734,597

Applicant(s)

POOL ET AL.

Examiner

Wanda M. Negrón

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on 03 August 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 23-25 is/are allowed.
- 6) ☒ Claim(s) 1-4, 7-9, 11, 12, 15, 16, 17 and 18-22 is/are rejected.
- 7) ☒ Claim(s) 5, 6, 10, 13 and 14 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

In view of the amendment filed on 8/3/2007, the objection to **claim 7** has been withdrawn.

Applicant's arguments, see page 6, with respect to **claim 7** have been fully considered and are persuasive. The 35 U.S.C. 112, second paragraph rejection of claim 7 has been withdrawn.

It is noted that the specification of the instant application recites on page 2, line 4 "*PCT/GB02/00138, filed July 14, 2002*", which does not correspond with the filing date of the published international application (WO 02/058157 A2), i.e. January 15, 2002.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4, 7-9, 11, 12, 15, 16, and 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burt et al. (EP Application Publication No. 0866501 A1), hereinafter referred to as Burt, and further in view of Kaplan (US Patent No. 5,867,215).

Regarding **claims 1 and 22**, Burt discloses a CCD imager (see figure 1) comprising a solid state imager arrangement comprising an image area (2), an output

register (4) which receives signal charge from the image area, a separate multiplication register (5) into which signal charge from the output register is transferred, means for obtaining signal charge multiplication by transferring the charge through a sufficiently high field in elements of the multiplication register (see col. 1, lines 48-55). Burt, however, fails to explicitly disclose an additional register into which excess signal charge is transferred.

Kaplan, on the other hand, discloses an image sensing device having a CCD chain, i.e. a CCD register, comprising elements 16 in figure 3 for removing charge exceeding a predetermine threshold (see abstract) in order to increase the dynamic range signal of each pixel (see col. 3, lines 16-19).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add an additional register, as disclosed by Kaplan, to the CCD imager taught by Burt in order to increase the dynamic range signal of each pixel.

Regarding **claim 2**, Burt as modified by Kaplan discloses that the excess signal charge is that exceeding a threshold level (see Kaplan, abstract).

Regarding **claim 3**, Burt as modified by Kaplan discloses that the threshold level is variable, i.e. the barrier 22 can be variable (see Kaplan, col. 5, lines 6-8) which, consequently, provides a variable threshold level.

Regarding **claim 4**, Burt as modified by Kaplan discloses that the excess signal charge is a percentage of the signal charge received from the image area, i.e. the excess charge overflowing barrier 22 into CCD wells 16 comprises a part of the entire signal charge received from the image area (see Kaplan, col. 4, lines 27-39).

Regarding **claim 7**, Burt as modified by Kaplan discloses that the signal charge from the output register is applied to a separator, i.e. barrier 22, which separates the excess signal charge from remaining signal charge, the excess charge being transferred to the additional register, i.e. CCD register formed by CCD wells 16 (see Kaplan, col. 4, lines 36-50), and that remaining signal charge to the multiplication register is transferred to the multiplication register (see Burt, col. 2, lines 30-33).

Regarding **claim 8**, Burt as modified by Kaplan discloses that the multiplication register has the same number of elements as the output register (see Burt, col. 3, lines 25-29). On the other hand, the additional register of Kaplan, i.e. CCD register formed by CCD wells 16, has the same number of elements as the output register (see Kaplan, figure 3), i.e. CCD register formed by CCD wells 14 which correspond with the output register of Burt. Therefore, it would be inherent that the multiplication register and the additional register have the same number of elements.

Regarding **claim 9**, Burt as modified by Kaplan discloses that the amount of excess charge transferred to the additional register, i.e. CCD register formed by CCD wells 16, is determined by implanted barrier means (see Kaplan, col. 5, lines 5-24).

Regarding **claim 11**, Burt as modified by Kaplan discloses a gate means, i.e. barrier 22 implemented as a "typical gate", for controlling the transfer of excess signal charge from the additional register, i.e. CCD register formed by CCD wells 16 (see Kaplan, col. 5, lines 5-24).

Regarding **claim 12**, Burt as modified by Kaplan discloses a means for combining (see Kaplan, figure 7) signal charge after it has been transferred through the multiplication register, i.e. the small CCD output register signal of Kaplan after it has been transferred to the multiplication register of Burt, with excess charge from the additional register, i.e. CCD register formed by CCD wells 16.

Regarding **claim 15**, Burt as modified by Kaplan discloses that a sufficiently high field region is obtained in each element of the multiplication register (see Burt, col. 2, line 57 - col. 3, line 1).

Regarding **claim 16**, Burt as modified by Kaplan discloses means for synchronizing signal readout from the multiplication register with line timing of a television rate signal (see Burt, col. 3, lines 22-29).

Regarding **claims 18 and 19**, Burt as modified by Kaplan discloses controlling the amplitude of one or more drive pulses applied to a register in order to control the amount of signal charge multiplication, and also discloses controlling the level of one or more dc potentials applied to a register to control the amount of signal charge multiplication (see Burt, col. 3, lines 44-56).

Regarding **claim 17**, Burt as modified by Kaplan discloses that the signal charge is clocked through the multiplication register at the same rate as charge is clocked through the output register (see Burt, col. 3, lines 20-22). Since the clocking rate of the additional register of Kaplan, i.e. CCD register formed by CCD wells 16, is associated with that of the output register, i.e. CCD register formed by CCD wells 14 of Kaplan (see col. 3, lines 2-8), it would be inherent that the multiplication register and the additional register are clocked at the same rate.

Regarding **claim 20**, Burt as modified by Kaplan discloses that the charge capacity of at least some of the elements of the multiplication register is larger than that of elements of the output register (see Burt, col. 3, line 57 – col. 4, line 7).

Regarding **claim 21**, Burt as modified by Kaplan discloses a plurality of multiplication registers arranged to receive signal charge from the output register (see

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Burt, col. 4, lines 14-18), at least one of the plurality having associated therewith an additional register, i.e. an anti-blooming structure (see Burt, col. 4, lines 8-13).

Allowable Subject Matter

Claims 5, 6, 10, 13 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding **claim 5**, the prior art fails to disclose, reasonably suggest or render obvious that ***the excess signal charge is transferred to the additional register via one or more elements of the multiplication register.***

Regarding **claim 6**, the prior art fails to disclose, reasonably suggest or render obvious that ***the excess signal charge is transferable from each element of the multiplication register to the additional register.***

Regarding **claim 10**, the prior art fails to disclose, reasonably suggest or render obvious that ***the barrier means is located between the multiplication register and the additional register.***

Regarding **claim 13**, the prior art fails to disclose, reasonably suggest or render obvious that the ***signal charge multiplication is obtained in the additional register.***

Regarding **claim 14**, the prior art fails to disclose, reasonably suggest or render obvious ***including a plurality of additional registers associated with the multiplication register.***

Claims 23-25 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding **claims 23-25**, independent claim 23 discloses a solid state imager arrangement comprising an image area, an output register which receives signal charge from the image area, a multiplication register comprising a plurality of multiplication elements into which signal charge from the output register is transferred for charge multiplication, an additional register comprising ***additional elements arranged to receive excess signal charge from the multiplication register***, and a clocking arrangement, wherein ***the clocking arrangement is arranged to clock the excess signal charge from the multiplication elements to corresponding ones of the additional elements***, which is which is neither taught or an obvious variation of the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's remarks with respect to the rejection of claims 1-12, 14-20 and 22-25 under 35 U.S.C. § 102(b) and 35 U.S.C. § 103(a) have been fully considered. It is noted that only references published more than one year before the US effective filing date of the present application, i.e. January 14, 2002, are available as a reference under 35 U.S.C. § 102(b). Therefore, the rejections have been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Burt et al. (EP Application Publication No. 0 866 501 A1), and further in view of Kaplan (US Patent No. 5,867,215). Since this is a new ground of rejection, which was not done because of an amendment, **this action is non-final**.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Hynecek (US Patent No. 5,337,340) discloses a CCD image sensor comprising a charge multiplier device.
- Spencer et al. (US Application Publication No. 2002/0093288 A1) teach an imaging apparatus comprising a CCD sensor including a multiplication register.

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- Nakashiba (US Patent No. 5,990,953) teaches a residual charge drain region and a potential barrier region.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wanda M. Negrón whose telephone number is (571) 270-1129. The examiner can normally be reached on Mon-Fri 6:30 am - 4:00 pm alternate Fri off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Wanda M. Negrón/

Examiner, Art Unit 2622
October 15, 2007



DAVID OMETZ
SUPERVISORY PATENT EXAMINER